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ANALYSIS OF A FILLING COPPER PILLAR BASED ON A THERMAL HOLE GLASS SUBSTRATE FOR A LED CHIP

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ABSTRACT

The glass substrate is drilled thermal holes by UV Laser and then is filled copper pillar on a thermal hole. The taper angles of 5o between top-side via hole and bottom-side via hole are 300 μm in thickness and 1 mm in length for a LED chip. The samples have the diameter/space ratio at 1/2 and 1/4 are fabricated by UV laser and the diameter of 100、200、300 μm. The made samples filled copper pillar model is used by numerical analysis. The minimum thermal conduction resistance is 3.178℃/W when a 2x2 array glass copper pillar substrate with 300 μm in diameter and 600 μm in spacing. By finite element method (FEM), the minimum thermal conduction resistance is 3.608℃/W at the same condition. Thermal conduction resistance of glass substrate is 214.2℃/W. The minimum thermal conduction resistance is decreased 98.5 % the thermal conduction resistance based on glass substrate. The numerical analysis results are similar with FEM simulated results. Its tolerance is almost 13.5 %.

KEYWORD: Laser Drilling, Thermal Hole, Finite Element Method (FEM), Numerical Analysis

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Research Article

INTRODUCTION

Light emitting diode (LED) is a semiconductor light device. For example, indoor/outdoor light, automotive light and backlight modules. Currently, photoelectric conversion efficiency for LED is almost 30 % [1]. Then, 60~70 % of the electric power is converted to thermal effect will cause junction temperature (Tj) to rise continuously. This effect affects the luminous power and LED lifetime. Therefore, heat management of LED and researching the heat dissipation materials are essential fields for future development [2-4].

Low Temperature Co-fired Ceramics (LTCC) with high thermal stability and excellent insulation can be used for LED substrate. LTCC has higher thermal conductivity of almost 3 ~ 4 W/m^{o}C [5] and LTCC are more expensive. In order to improve the shortcomings of the substrate, specifically in its low thermal stability and high cost, glass substrate can be used as heat dissipation substrate for LED [6,7]. Furthermore, the coefficient thermal expansion (CTE) of glass is similar to silicon substrate. However, this glass has good insulation and optical transmission. Therefore, we choose the glass substrate as a heat dissipation substrate of the LED through chip on board (COB) [8]. In order to increase the heat dissipation ability of glass substrate, laser can be employed to create thermal vias [9], and filling copper pillar based on a thermal via hole glass substrate for a LED chip. Copper is filled in the hole will be effective reducing the thermal resistance of the glass substrate. This paper uses numerical analysis model to calculate this via hole in diameter and in space of the glass substrate resistance. Its optimization of glass substrate thermal resistance and verification of result is done through FEM simulation [10].

UV LASER DRILLING AND NUMERICAL ANALYSIS

Glass substrate is drilled 100, 200, 300 □m diameter and diameter (d)/space (p) of 1/2 and 1/4 with the thicknesses of 300 □m. UV Laser is used to drill the glass substrate with a wavelength of 355 nm and an optical power of 1.5W by Hyper Diamond UV. The samples are fabricated to these square symmetric array thermal holes with a nominal hole diameter of 100、200、300 μm and the diameter/space of 1/2 and 1/4 based on 1mm X 1mm glass substrate for a LED chip area. Figure 1(a) UV laser is drilling on top-side of glass substrate 1(b) UV laser is drilling on bottom-side of glass substrate. Hole diameter have three kind of 100、200 and 300 μm. 1(c) is the taper angles of 5^{o} between top-side via hole and bottom-side via hole are 300 μm in thickness, Figure 2(a) Three kind of diameter/space ratio is 1/2 including 100 μm in diameter、200 μm in space of the 5X5 array thermal hole glass substrate, 200 μm in diameter、400 μm in space of the 3X3 array thermal hole glass substrate and 300 μm in diameter, 600 μm in space of the 2X2 array thermal hole glass substrate. 2(b)Glass substrate are two kind of hole diameter/space of 1/4, One is 100 μm in diameter、400 μm in space of the 3X3 array thermal hole glass substrate and anther is 200 μm in diameter、800 μm in space of 2X2 array thermal hole glass substrate.

Figure 1: Laser Drilled in 300 μm in Thickness on Glass Substrate. (a)Top-Side (b) Bottom-Side (c)Schematic Diagram of Top-Side and Bottom-Side via Hole

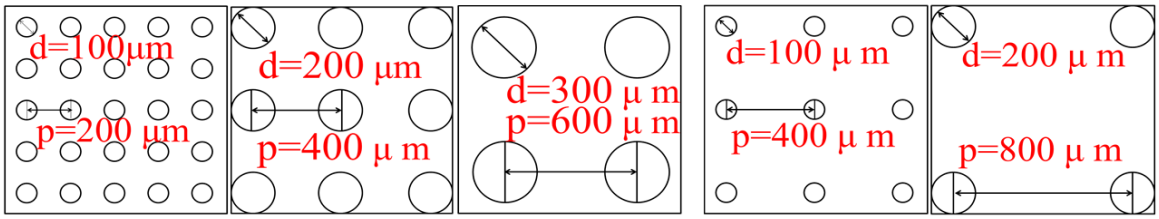

Figure 2: Array Thermal Hole Glass Substrate of the Diameter/Space ratio. (a) d/P=1/2 via Hole on Glass Substrate(b)d/p=1/4 Thermal Hole Glass Substrate

Numerical analysis model for the thickness (t) of 300 μm in glass substrate is calculated with thermal conduction resistance. Thermal radiation is negligible as the operating temperature of LED generally is less than 300^{o}C. LED chip dimension is 1mm x 1mm, and the hole diameter (d) range for heat dissipation of glass substrate is set to 52.5 μm ~ 350

μm and taper angles of 5°. The array thermal hole glass substrate have the diameter/space ratio at 1/2 and 1/4 includes 2X2、3X3 and 5X5 array thermal hole glass substrate. Figure 3 is a model for effective thermal conduction resistance of thermal hole glass substrate with 5° in taper angles. Thermal conduction resistance (R_{cond}) can be found by considering glass area thermal conduction resistance (R_g) and copper based thermal conduction resistance (R_{cu}) to be in parallel as shown in equation (1).

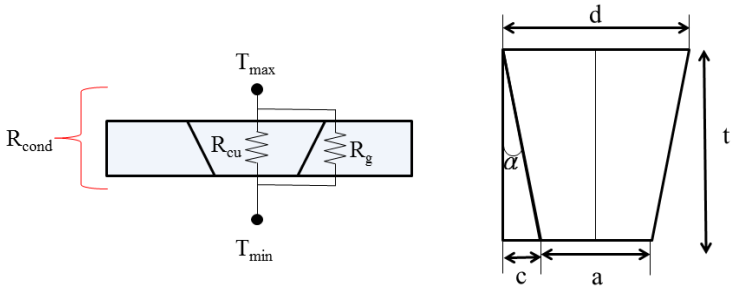

Figure 3: Diagram Showing the Effective Thermal Conduction Resistance of Hole Array Glass Substrate

$$R_{cond} = \frac{1}{\frac{1}{R_{cu}} + \frac{1}{R_g}} \tag{1}$$

Thermal conduction resistance of the heat dissipating substrate is directly proportional to its thickness, and inversely proportional to its surface area. The thermal conduction resistance in Copper (R_{cu}) based on a array thermal hole glass substrate is usually equivalent to the thickness of substrate (t) divided by the thermal conductivity of copper (K_{cu}), where K_{cu} is 400 W/m°C as shown in equation (2). Glass area thermal conduction resistance (R_g) is obtained by dividing the thickness of substrate with the product of total area of glass substrate (subtract the total area of holes from the area of glass substrate) and thermal conductivity of glass (K_g) is 1.4 W/m°C as shown in equation (3). Equation 4 shows the expanded equation to calculate thermal resistance due to conduction in array thermal hole glass substrate.

$$R_{cu} = \int_0^t \frac{1}{R_{cu} \cdot N^2 \cdot \frac{\pi(d - 2 \cdot t \cdot \tan 5^o)^2}{4}} dt \tag{2}$$

$$R_g = \int_0^t \frac{1}{k_g \cdot N^2 \cdot \left(p^2 - \frac{\pi\left(d - 2 \cdot t \cdot \tan 5^o\right)^2}{4} \right)} dt \tag{3}$$

$$R_{cond} = \int_0^t \frac{1}{k_{cu} \cdot N^2 \cdot \frac{\pi\left(d - 2 \cdot t \cdot \tan 5^o\right)^2}{4} + k_g \cdot N^2 \cdot \left(p^2 - \frac{\pi\left(d - 2 \cdot t \cdot \tan 5^o\right)^2}{4} \right)} dt \tag{4}$$

Figure 4 shows numerical analysis of different trends in thermal conduction resistance of array thermal hole glass substrate with 300 μm in thickness、1 mm in length and taper angles 5° of glass substrate. Figure 4 shows trend in thermal

conduction resistance in 2X2、3X3 and 5X5 array thermal hole glass substrates. As the hole diameter increases from 52.5 to 350 μm, thermal conduction resistance due to heat conduction in 2X2、3X3、5X5 array increase. When hole diameter is fixed at 100 μm to observe the difference in thermal conduction resistance of via arrays, it can be concluded that as the number of array increases, the thermal conduction resistance decrease.

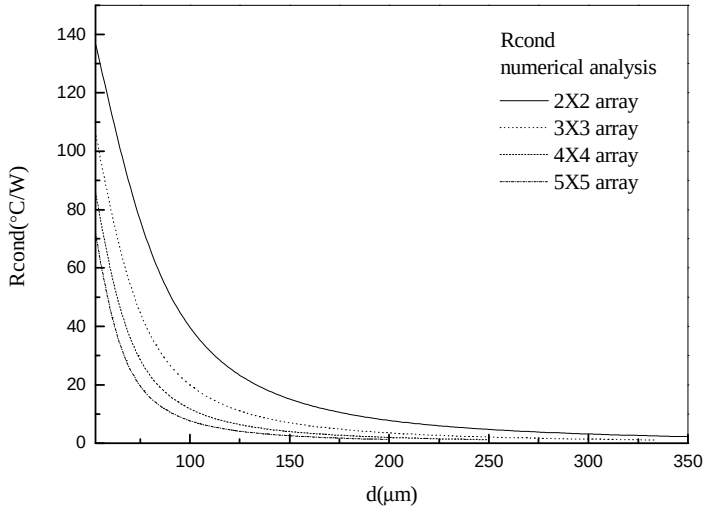

Figure 4: Thermal Conduction Resistance of Glass Substrates with the Diameter of 2x2、3x3、5x5 Hole Array

FINITE ELEMENT METHOD

Ansys software is used to perform FEM simulation of steady-state heat distribution of array thermal hole glass substrate with 300 μm in thickness and 1 mm in length and 5^{o} in taper angles of hole filled copper based on a thermal hole glass substrate. The array thermal hole glass substrate are including 2X2、3X3、5X5 array and diameter of 100、200 and 300 μm. The thermal hole glass substrate have the diameter/space ratio at 1/2 and 1/4. To simulate steady-state heat distribution, base plate thermal power of the glass substrate is set as 1 W while the ambient temperature of upper plate are set at 25 ^{o}C. R_{cond} is equal to maximum temperature (T_{max}) minus minimum temperature (T_{min}) and divide the result by thermal power (W). Figure 5(a) shows the steady-stead heat distribution result using FEM to perform steady-state thermal simulation of glass with 300 μm in thickness of glass and 1 mm in length of glass, and its R_{cond} is 214.29 ℃/W. Figure 5(b) shows the cross section of heat distribution in glass hole substrate. Figure 5(c) shows 2X2 array thermal hole glass substrate with diameter of 300 μm and space of 600 μm, and the steady-state thermal simulation result reveals its R_{cond} to be 3.608 ^{o}C/W. Figure 5(d) shows the cross section of heat distribution in 2X2 array thermal hole glass substrate. When Ansys performs simulation for different hole arrays with different hole diameters, R_{cond} shows a significant decreasing trend as compared to glass substrate. Currently, simulation result only show the steady-state heat distribution of minimum R_{cond} while R_{cond} of other simulation results are summarized in Table 1.

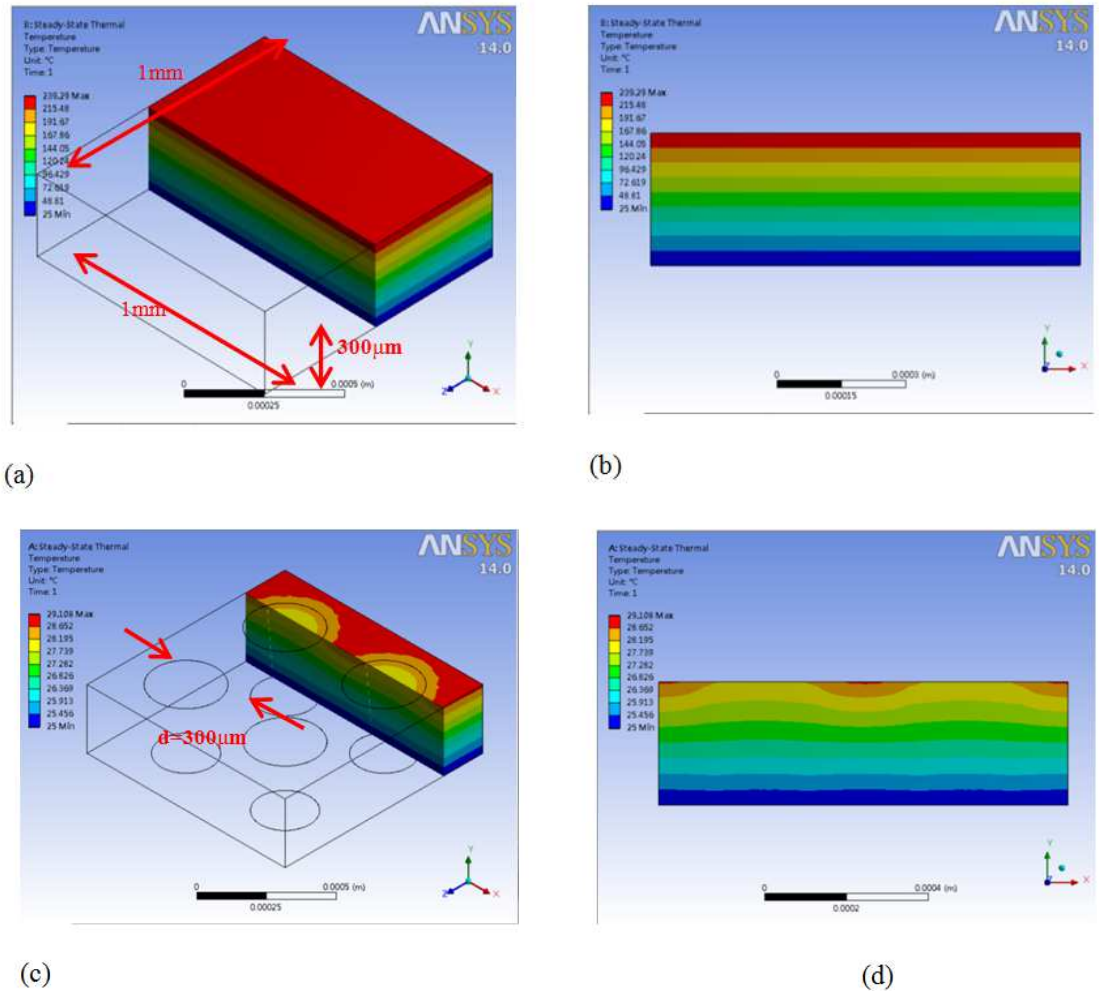

Figure 4: Steady-State Heat Distribution of Array Thermal Hole Glass Substrate Sample with Thickness of 300 μm and Length of 1 mm using FEM Simulation (a) Steady-State Thermal Simulation Result of Glass Substrate; (b) Side View of Heat Distribution of Steady-State Thermal Simulation Performed on Glass Substrate (c) Steady-State Heat Distribution Result of 2x2 via Array Glass Substrate with d of 300 μm and p of 600 μm; (d) Side View Steady-State Thermal Simulation Heat Distribution Performed on 2x2 via Array Glass Substrate

. Table 1 shows the comparison between tolerance of R_{cond} values obtained through numerical analysis and FEM simulation performed on array thermal hole glass substrates with d being (a) 100、200、300 μm (b) the optimal value (also known as the minimum value). 2X2 array yields the maximum tolerance of about 13.5% between R_{cond} obtained through numerical analysis and that obtained through FEM simulation under the conditions of 300 μm in hole diameter and 600 μm in hole spacing. The corresponding R_{cond} obtained from numerical analysis and FEM simulation are 3.178 ℃/W and 3.608 ℃/W respectively. the R_{cond} of 2X2 array thermal hole glass substrate is lower than that of glass substrate without pores by 98.5%. As a result, it can be concluded that numerical analysis and FEM simulation yields highly similar R_{cond} values for glass substrates with various via arrays

Table 1: Comparison between R_{cond} Obtained through Numerical Analysis and FEM Stimulation Performed on Single via and other via Array Glass Substrate

Via Parameters		Thermal Resistance		Rate of Reducing R_{cond}(%)		Error (%)
Array	Dia. (μm)	Spacing (μm)	R_{cond} (℃/W)	FEM (℃/W)		$\left\|\frac{R_{cond}-FEM}{R_{cond}}\times 100\%\right\|$
No via	0	0	214.28	214.29	0	0.004
2x2	200	800	7.816	8.74	96.3	11.8
	300	600	3.178	3.608	98.5	13.5
3x3	100	400	20.518	21.006	90.5	2.4
	200	400	3.548	3.804	98.3	7.2
5x5	100	200	7.957	8.09	96.3	1.7

RESULTS AND DISCUSSIONS

Figure 6 shows the analysis of R_{cond} obtained through numerical analysis and FEM simulation performed on array thermal hole glass substrate with 300 μm in thickness of glass substrate and 1 mm in length of glass substrate thickness of 300 μm and length of 1mm. The solid/dotted lines are R_{cond} obtained through numerical simulation of 2X2、3X3、5X5 array thermal hole glass substrates and diameter of 100、200、300 μm while the different markings represent R_{cond} obtained through FEM stimulation. Result from both the numerical analysis model constructed in this paper and FEM simulation by Ansys software shows similar curved result.

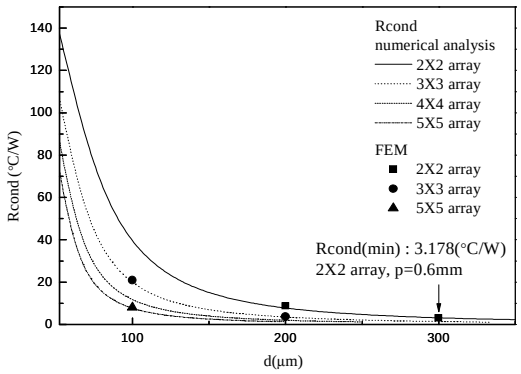

Figure 6: Thermal Conduction Resistance (R_{cond}) is Obtained by Numerical Analysis and FEM Based on Single via and 2x2、3x3、5x5 Array Thermal Hole Glass Copper Pillar Substrate with 300 μm in Thickness and 1 mm in Length

CONCLUSIONS

The glass substrate is drilled thermal holes by UV Laser and then is filled copper pillar on a thermal hole. The taper angles of 5^o between top-side via hole and bottom-side via hole are 300 μm in thickness and 1 mm in length for a

LED chip. The samples have the diameter/space ratio at 1/2 and 1/4 are fabricated by UV laser and the diameter of 100、200、300 μm. Numerical analysis model applied on 2X2 array thermal hole substrate with 300 μm in hole diameter, 600 μm in hole space, 300 μm in thickness of glass substrate, 1 mm in length and filling copper pillar based of glass substrate yields a minimum R_{cond} of 3.178 ^{o}C/W. In addition, when FEM simulation is performed on identical glass substrates with condition of 2X2 array with 300 μm in via diameter and 600 μm in space, the tolerance between FEM simulation and numerical analysis is max. 13.5 %. This verifies that the distribution of total thermal resistance obtained through numerical analysis model constructed in this paper is almost identical to that obtained through FEM simulation.

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